



Version with markings to show changes made

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/652,550
Filing Date August 31, 2000
Inventor Keiji Jono et al.
Assignee Micron Technology, Inc. and KMT Semiconductor, LTD
Group Art Unit 2811
Examiner T. Tran
Attorney's Docket No. KM1-001
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods
of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods
of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated
Transistor, Trench Isolation Structures Formed in a Semiconductor,
Memory Cells and DRAMS

37 CFR § 1.121(b)(1)(iii) AND 37 CFR § 1.121(c)(1)(ii)
FILING REQUIREMENTS TO ACCOMPANY RESPONSE TO
OCTOBER 12, 2001 OFFICE ACTION

Deletions are bracketed, additions are underlined.

In the Claims

Claims 33-61 have been canceled.

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